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10/710,012	06/11/2004	Chien-Chao Huang	2001.1531 / 24061.439	4011

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EXAMINER
ISAAC, STANETTA D

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 03/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/710,012	HUANG ET AL.	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13,14,27 and 28* is/are allowed.

6)☒ Claim(s) *2-12 and 15-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the amendment filed on 1/09/06. Currently, claims 2-29 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 2-8, 10, 15, 17-23 and 29 are rejected under 35 U.S.C. 102(b) as being anticipated by Yeo et al., US Patent 6,492,216 (Embodiment 2).

Yeo discloses the semiconductor method as claimed. See figures 1-5, 7 and 8 (Embodiment 2), and corresponding text, where Yeo teaches, pertaining to claim 6, a method comprising: providing a semiconductor alloy layer **2** on a semiconductor substrate **1** (figure 1; col. 3, lines 32-65); forming a gate structure **6** on the semiconductor alloy layer **2** (figure 4; col. 4, lines 57-62); forming source and drain regions **7** in the semiconductor substrate **1** on both sides of the gate structure (figure 5; col. 4, lines 63-67; col. 5, lines 1-25); removing at least a portion of the semiconductor alloy layer overlying the source and drain regions (figure 7; col. 5, lines 44-54); and forming a metal silicide region **10** over the source and drain regions (figure 8; col. 5, lines 54-62); wherein removing at least a portion of the semiconductor alloy layer comprises: altering at least a portion of the semiconductor alloy layer to a material receptive to a selective removal process (col. 5, lines 50-54); and selectively removing the altered

semiconductor alloy layer form overlying the source and drain regions (figure 7; col. 5, lines 50-54). In addition, Yeo teaches, pertaining to claim 2, wherein the selectively removing comprises etching the altered semiconductor alloy layer (figure 7; col. 5, lines 50-54). Also, Yeo teaches, pertaining to claim 3, wherein the selectively removing comprises exposing the altered semiconductor alloy layer to an etchant for a period of time until the altered semiconductor alloy layer overlying the source and drain regions is fully removed (figure 7; col. 5, lines 46-54). Yeo teaches, pertaining to claim 4, wherein the forming a metal silicide region comprises forming a metal silicide region having a metal selected from the group consisting of cobalt and titanium (col. 5, lines 25-42). In addition, Yeo teaches, pertaining to claim 5, wherein removing the altered semiconductor alloy layer comprises using an anisotropic reaction ion etch (col. 5, lines 50-54). In addition, Yeo teaches, pertaining to claim 7, wherein the altering includes oxidizing at least a portion of the semiconductor alloy layer to form a silicon oxide material receptive to a selective wet etch process (figure 4; col. 3, lines 65-67; col. 4, lines 41-62, ***Note***: the Examiner takes the position that the optional capping layer is not used); and wherein the selectively removing includes removing the altered semiconductor alloy layer from overlying the source and drain regions (col. 4, lines 57-62). Also, Yeo teaches, pertaining to claim 8, wherein the altering includes oxidizing at least a portion of the semiconductor alloy layer to form a silicon oxide material receptive to a selective dry etch process (figure 4; col. 3, lines 65-67; col. 4, lines 41-62, ***Note***: the Examiner takes the position that the optional capping layer is not used); and wherein the selectively removing includes removing the altered semiconductor alloy layer from overlying the source and drain regions (col. 4, lines 53-57). Yeo teaches, pertaining to claim 10, wherein the altering includes consuming at least a portion of the semiconductor alloy layer to form a

metal silicide material receptive to a selective dry etch process (figure 8; col. 5, lines 44-62); and wherein selectively removing includes removing the altered semiconductor alloy layer from overlying the source and drain regions (col. 5, lines 50-54). Pertaining to claim 15, Yeo teaches, wherein the semiconductor alloy layer comprises SiGe (col. 3, lines 30-60). Finally, Yeo teaches, pertaining to claim 16, wherein anneal the metal layer comprises performing a rapid thermal anneal process (col. 5, lines 30-35).

Yeo teaches, pertaining to claim 17, Yeo teaches, wherein a method of forming a semiconductor device, comprising: forming a gate structure **6** on a semiconductor alloy layer **2** in a semiconductor substrate **1** (figure 1; col. 3, lines 32-65); forming source and drain regions **7** in the semiconductor substrate on both sides of the gate structure (figure 5; col. 4, lines 63-67; col. 5, lines 1-25); altering at least a portion of the semiconductor alloy layer overlying the source and drain regions (figure 7; col. 5, lines 44-54); and removing, at least partially, the altered semiconductor alloy layer overlying the source and drain regions (figure 7; col. 5, lines 44-54). In addition, Yeo teaches, pertaining to claim 18, further comprising forming a metal silicide layer over the source and drain regions **10** (figure 8; col. 5, lines 54-62). Also, Yeo teaches, pertaining to claim 19, wherein removing the altered semiconductor alloy layer comprises etching the semiconductor alloy (figure 7; col. 5, lines 44-54). Yeo teaches, pertaining to claim 20, wherein removing the altered semiconductor alloy layer comprises exposing the altered semiconductor alloy layer to an etchant for a period of time until the semiconductor alloy layer overlying the source and drain regions is fully removed (figure 7; col. 5, lines 44-54). In addition, Yeo teaches, pertaining to claim 21, wherein forming a metal silicide region comprises forming a metal silicide region having a metal selected from the group consisting of cobalt and

titanium (col. 5, lines 25-42). Also, Yeo teaches, pertaining to claim 22, wherein removing the altered semiconductor alloy layer comprises using an anisotropic reaction ion etch to remove at least a portion of the altered semiconductor alloy layer (col. 5, lines 45-54). Yeo teaches, pertaining to claim 23, wherein altering and removing at least a portion of the semiconductor alloy layer comprises: oxidizing at least a portion of the semiconductor alloy layer to form a silicon oxide material receptive to selective etch process (figure 4; col. 3, lines 65-67; col. 4, lines 41-62, ***Note***: the Examiner takes the position that the optional capping layer is not used); and selectively removing the altered semiconductor alloy layer from overlying the source and drain regions (col. 4, lines 57-62). Finally, Yeo teaches, pertaining to claim 29, wherein the semiconductor alloy layer comprise SiGe (col. 3, lines 30-60).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9, 11, 12, 24, 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeo et al., US Patent 6,492,216 (Embodiment 1) in view of Nagabushnam US Patent 6,171,959 .

Yeo discloses the semiconductor method substantially as claimed. See preceding rejection of claims 2-8, 10, 15, 17-23 and 29 (Embodiment 2) under 35 U.S.C. 102(b).

However, Yeo fails to show in (Embodiment 2), pertaining to claim 9, wherein removing at least a portion of the semiconductor alloy layer comprises: consuming at least a portion of the semiconductor alloy layer to form a metal silicide material receptive to a selective wet etch process; and selectively removing the altered semiconductor alloy layer from overlying the source and drain regions. In addition, Yeo fails to show in (Embodiment 2), pertaining to claim 11, wherein removing at least a portion of the semiconductor alloy layer comprises: forming a metal layer over the semiconductor alloy layer overlying the source and drain regions; annealing the metal layer and the semiconductor alloy layer and forming a metal silicide material; and selectively etching the metal silicide material. Also, Yeo fails to show in (Embodiment 2), pertaining to claim 24, wherein altering and removing at least a portion of the semiconductor alloy layer comprises: consuming at least a portion of the semiconductor alloy layer to form a metal silicide material receptive to a selective etch process; and selectively removing the altered semiconductor alloy layer from overlying the source and drain regions. Finally, Yeo fails to show in (Embodiment 2), pertaining to claim 25, wherein altering and removing at least a portion of the semiconductor alloy layer comprises: forming a metal layer rover the semiconductor alloy layer overlying the source and drain regions; annealing the metal layer and the semiconductor alloy layer and forming a metal silicide material; and selectively etching the metal silicide material.

Yeo teaches in figures 1-5 and 6 (Embodiment 1), and correspond text, pertaining to claim 9, wherein removing at least a portion of the semiconductor alloy layer comprises: consuming at least a portion of the semiconductor alloy layer to form a metal silicide material receptive to a selective wet etch process (figure 6; col. 5, lines 25-43); and selectively removing

the altered semiconductor alloy layer from overlying the source and drain regions (col. 5, lines 25-43). In addition, Yeo teaches (Embodiment 1), pertaining to claim 11, wherein removing at least a portion of the semiconductor alloy layer comprises: forming a metal layer over the semiconductor alloy layer overlying the source and drain regions (figure 6; col. 5, lines 25-43); annealing the metal layer and the semiconductor alloy layer and forming a metal silicide material **10** (col. 5, lines 30-35); and selectively etching the metal silicide material (col. 5, lines 35-43). Also, Yeo teaches (Embodiment 1), pertaining to claim 12, wherein removing at least a portion of the semiconductor alloy layer comprises: forming a metal layer over the semiconductor alloy layer overlying the source and drain regions (figure 6; col. 5, lines 25-43); annealing the metal layer and the semiconductor alloy layer and forming a disposable metal silicide material **10** (col. 5, lines 30-35); selectively etching the disposable metal silicide material overlying the source and drain regions (col. 5, lines 35-43). Yeo teaches (Embodiment 1), pertaining to claim 24, wherein altering and removing at least a portion of the semiconductor alloy layer comprises: consuming at least a portion of the semiconductor alloy layer to form a metal silicide material receptive to a selective etch process (figure 6; col. 5, lines 25-43); and selectively removing the altered semiconductor alloy layer from overlying the source and drain regions (col. 5, lines 25-43). In addition, Yeo teaches (Embodiment 1), pertaining to claim 25, wherein altering and removing at least a portion of the semiconductor alloy layer comprises: forming a metal layer rover the semiconductor alloy layer overlying the source and drain regions (figure 6; col. 5, lines 26-30); annealing the metal layer and the semiconductor alloy layer and forming a metal silicide material (col. 5, lines 30-35); and selectively etching the metal silicide material (col. 5, lines 35-43). Finally, Yeo teaches (Embodiment 1), pertaining to claim 26, wherein altering and

removing at least a portion of the semiconductor alloy layer comprises: forming a metal layer over the semiconductor alloy layer overlying the source and drain regions (figure 6; col. 5, lines 25-43); annealing the metal layer and the semiconductor alloy layer and forming a disposable metal silicide material **10** (col. 5, lines 30-35); selectively etching the disposable metal silicide material overlying the source and drain regions (col. 5, lines 35-43).

Nagabushnam, teaches, in figures 1-8, and corresponding text, forming a second metal layer and annealing the second metal layer to form a second silicide (col. 5, lines 34-67).

It would have been obvious to one of ordinary skill in the art to incorporate the follow steps of: wherein removing at least a portion of the semiconductor alloy layer comprises: consuming at least a portion of the semiconductor alloy layer to form a metal silicide material receptive to a selective wet etch process; and selectively removing the altered semiconductor alloy layer from overlying the source and drain regions; wherein removing at least a portion of the semiconductor alloy layer comprises: forming a metal layer over the semiconductor alloy layer overlying the source and drain regions; annealing the metal layer and the semiconductor alloy layer and forming a metal silicide material; and selectively etching the metal silicide material; wherein altering and removing at least a portion of the semiconductor alloy layer comprises: consuming at least a portion of the semiconductor alloy layer to form a metal silicide material receptive to a selective etch process; and selectively removing the altered semiconductor alloy layer from overlying the source and drain regions; wherein altering and removing at least a portion of the semiconductor alloy layer comprises: forming a metal layer rover the semiconductor alloy layer overlying the source and drain regions; annealing the metal layer and

the semiconductor alloy layer and forming a metal silicide material; and selectively etching the metal silicide material, in the method of Yeo (Embodiment 2), pertaining to claims 9, 11, 24 and 25, according to the teachings of Yeo (Embodiment 1), with the motivation that, since both Embodiments 1 and 2 teach the subsequent formation of metal silicide regions, where a conventionally known advantage is to provide lowered resistance. Therefore, whether the metal silicide regions are formed by the process of Embodiment 1 or 2, would prove to be equivalent since ultimately the goal is to provide the source/drain regions with metal silicide regions.

It would have been obvious to one of ordinary skill in the art, to incorporate, the steps of: forming a second metal layer; and annealing the second metal layer and forming a second metal silicide material, in the method of Yeo, pertaining to claims 12 and 26, according to the teachings of Nagabushnam, with the motivation that, by including an additional metal layer to form silicide regions will help improve the conventional advantages of having a lower resistivity, thereby improving the ohmic contact of the source/drain regions.

Allowable Subject Matter

Claims 13, 14, 27 and 28 are allowed over the prior art of record.

The following is an examiner's statement of reasons for allowance:

The closest prior art of record, Yeo et al., US Patent 6,492,216 alone or in combination with Yeo et al., US Patent 6,492,216 in view of Nagabushnam US Patent 6,171,959, fails to show, the steps of:

Pertaining to claims 13 and 27, "implanting ions of at least one predetermined species into at least a portion of the metal-semiconductor alloy layer;"

Pertaining to claims 14 and 28, "implanting ions of at least one predetermined species into at least a portion of the metal layer;"

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

Applicant's arguments, see Remarks, filed 1/06/06, with respect to the rejection(s) of claim(s) 2-29 under 102(b) and 103(a), respectively have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Yeo et al., US Patent 6,492,216 (**Embodiment 2**) under 102(b), and Yeo et al., US Patent 6,492,216 (Embodiment 1) in view of Nagabushnam US Patent 6,171,959 under 103(a).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stanetta Isaac
Patent Examiner
March 20, 2006

MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER